

10/6 44, 45-4

example, another type of memory device such as an SRAM, DRAM and other volatile or non-volatile memories, as well as other integrated circuit devices for examples, a microprocessor, digital signal processor (DSP), application specific integrated circuit (ASIC) and programmable devices such as a field programmable gate array (FPGA) and a programmable logic device (PLD).

[0048] Programmable delay circuit 515 includes program register 560 and delay selection circuitry 541. Delay selection circuitry 541 includes decoder 555, multiplexer 550, and 2^n delay paths including delay path 571 and 2^n-1 delay paths including delay elements 572-579 to delay the reference clock signal 438 by different time periods. More or less delay elements may also be used. In one embodiment, for example, a delay element may be a series of one or more inverters (e.g., inverter 781) as illustrated by delay element 770 of Figure 7. Alternatively, other types of delay elements may be used, for examples, buffers and RC network components. Programmable delay circuit 515 also includes a delay path 571 that is limited only by the intrinsic impedance of the conductive trace of the path.

[0049] Each of delay elements 572-579 are coupled to receive CLK reference signal 438 and generate a correspondingly delayed internal clock signal that is output to multiplexer 550. Each of delay elements 572-579 may provide a different time period delay. For example, delay element 571 represents a direct connection between reference clock signal 438 and multiplexer 550 (i.e., no delay

10/644,454

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Date: January 3, 2005

Re: **Application Serial No. 10/644,454**
Atty Docket No. 02489.P035D

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1. Copy of Page 20 of above-identified application (1 Page)

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